WHITE PAPER

FlexRay Physical Layer Waveform Analysis SI Voting Procedures

SB5000 Vehicle Serial Bus Analyzer

QUALITY ■ INNOVATION ■ FORESIGHT

YOKOGAWA

WP 7013-61E

Introduction

"FlexRay" is the latest in-vehicle communication system developed to provide a deterministic and fault-tolerant bus system with high data rates for advanced automotive control applications. The FlexRay Consortium (FRC) is responsible for creating and maintaining the specifications of FlexRay and the Physical Layer Working Group is currently developing an "SI (System Integrity) Voting Procedure" in order to ensure that the Electrical Physical Layer performs correctly. This white paper describes an easy method of testing according to the requirements provided from the FlexRay Consortium Physical Layer Working Group with the aim of analyzing Signal Integrity in different bus topologies.

What is the "SI Voting Procedure" ?

The aim of the signal integrity voting procedure is to detect whether a FlexRay bus topology is operable in principle or not and follows the properties of the Bus Driver (BD) and its robustness against disturbances. For simplicity, the wave shape of a single bit is examined, which has to be preceded by three inverted bits and followed by one inverted bit.

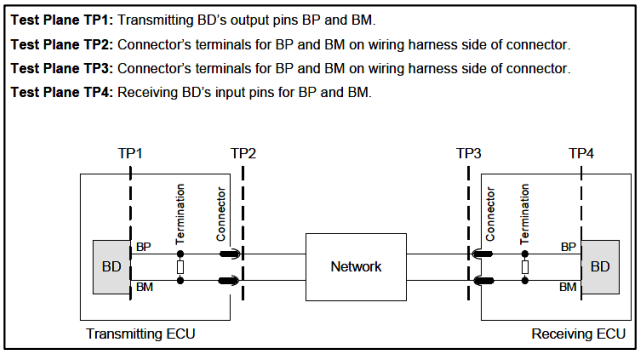
Why is the SI Voting Procedure required ?

Analysis of the signal's eye diagram is assumed to be the normal method for evaluating the FlexRay physical layer. However in the case of passive networks, communication can work faultlessly but failure of the eye diagram test is possible due to signal reflections.

SI Voting is being proposed to analyze the physical layer to counter this problem. Generally, the eye diagram is being considered as a the primary test, and the SI Voting Procedure as a secondary test for evaluating the physical layer. When the eye diagram test results in failure, the SI Voting procedure would be used to examine the reasons.

Test procedures and the criteria

The shape of the differential bus signal at a test plane (TP1 to TP4) is examined (Figure 1.)



<Figure 1> Test Planes

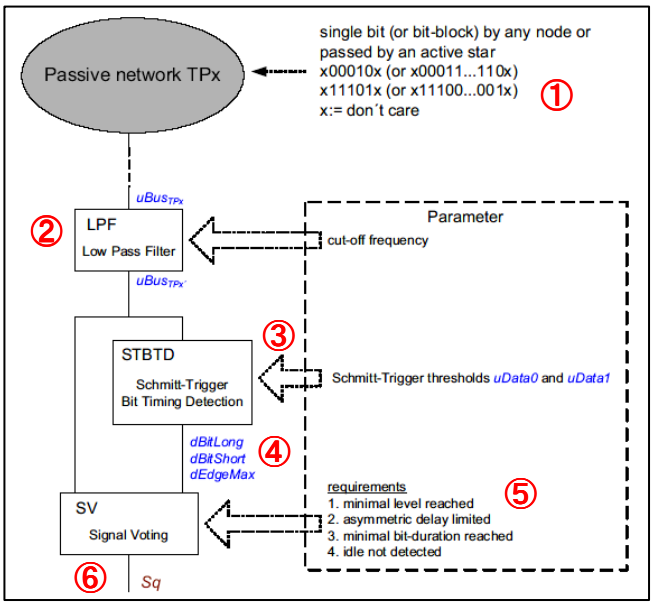
Source:
FlexRay Communications System
Electrical Physical Layer Specification
Version 2.1 Revision B

The following four(4) criteria must all be satisfied in order to pass the SI Voting test.

1. The differential voltage level must exceed the criteria.
2. Asymmetry must be within a permissible range.
3. Bit length (duration) must be sufficient.
4. Idle (Note 1, see below) is not detected.

Note 1:
The test signal may not remain in the range of +/- 300mV(uData1(max) and uData0(min)) longer than 50ns (minimum allowable idle time).

The test procedure (flow chart) is shown in figure 2.



<Figure 2> Single bit signal integrity model

① In a passive network TPx, the following single bit (or bit-block) from any node or passed by an active star is the test target signal (uBustpx).

x00010x
x11101x
(x: Don't care)

② The uBustpx passes a mathematical low-pass filter (Note 2).

Note 2: 1st order, the cut off Frequency is 14MHz(-3dB)

③ The filtered signal (uBustpx') passes a Schmitt-Trigger with the threshold variations according to Figure 3. Each bit duration according to the threshold variations is measured.
Also, edge durations (dEdge10 for falling edge, dEdge 01 for rising edge) are measured. (Figure 4).

④ The shortest detectable duration of one bit (dBitShort), the longest detectable duration of one bit (dBitLong) and the detected duration of the slowest edge (dEdgeMax: MAX(dEdge01, dEdge10) are identified from the result of step "③".

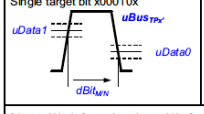
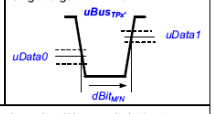
⑤ All parameters measured above must meet the following criteria.

1. The differential voltage level has to be high (or low) enough. (uBustpx' must be higher than "uData1Top" (or lower than "uData0Top")

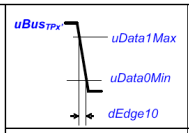
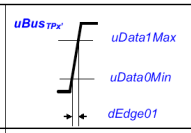
2. The asymmetry of the measured bit has to be less than the limit. ("dBitLengthVariation": dBitLong – dBitShort must be less than the criteria of "dBitLengthVariation Max".)

3. The shortest detectable duration of one bit has to be long enough. ("dBitShort" must be longer than the criteria of "dBitMin".)

4. Idle must not be detected during the frame. ("dEdgeMax" must be longer than the criteria of "didleDetectionMin".)

BEHAVIOR bit-length	Single target bit x00010x  	Single target bit x11101x  		Duration of one single *Data_0* or *Data_1* bit measured at different thresholds.
3 inverted bits before and one inverted bit after the monitored bit are required at least				
uData1	*uData0*	*uData0*	*uData1*	
300mV	-300mV	-300mV	300mV	$dBit_{300:300}$
300mV	-270mV	-270mV	300mV	$dBit_{300:270}$
270mV	-300mV	-300mV	270mV	$dBit_{270:300}$
270mV	-240mV	-240mV	270mV	$dBit_{270:240}$
240mV	-270mV	-270mV	240mV	$dBit_{240:270}$
240mV	-210mV	-210mV	240mV	$dBit_{240:210}$
210mV	-240mV	-240mV	210mV	$dBit_{210:240}$
210mV	-180mV	-180mV	210mV	$dBit_{210:180}$
180mV	-210mV	-210mV	180mV	$dBit_{180:210}$
180mV	-150mV	-150mV	180mV	$dBit_{180:150}$
150mV	-180mV	-180mV	150mV	$dBit_{150:180}$
150mV	-150mV	-150mV	150mV	$dBit_{150:150}$
180mV	-180mV	-180mV	180mV	$dBit_{180:180}$
210mV	-210mV	-210mV	210mV	$dBit_{210:210}$
240mV	-240mV	-240mV	240mV	$dBit_{240:240}$
270mV	-270mV	-270mV	270mV	$dBit_{270:270}$

<Figure 3> Signal Voting –bit length measurements

BEHAVIOUR edge-duration	$uBus_{TPx'}$  	$uBus_{TPx'}$  	Determination of edge durations	
	uData1Max = 300mV	*uData1Max* = 300mV		
	uData0Min = -300mV	*uData0Min* = -300mV	*dEdge10*	*dEdge01*

<Figure 4> Signal Voting –edge duration measurements

⑥ The test is judged as "Sq=pass" when all criteria described at "⑤" are satisfied. Otherwise it is judged as "Sq=fail".

Figures 5 and 6 show the explanation for each parameter.

dBitLengthVariation	detected length variation
dBitLengthVariation Max	allowed maximal length variation
dBitMin	allowed shortest Bit at TP4_BDi (e.g. limited by the properties of the CC)
dBitLong	shortest detectable duration of one bit
dBitShort	longest detectable duration of one bit
$uBus_{TPx}$	differential voltage at any test plane
$uBus_{TPx'}$	filtered differential voltage $uBus_{TPx'}$
uData0Top	required voltage $uBus_{TPx'}$ to detect *Data_0*
uData1Top	required voltage $uBus_{TPx'}$ to detect *Data_1*
dIdleDetectionMin	minimal timeout to detect *Idle*
dEdgeMax	detected duration of the slowest edge
Sq	voted signal quality: "*pass*" or "*fail*" Fail: the signal shape does not meet the specified requirements Pass: the signal shape meets the specified requirements system specific individual additional voting states like e.g. "warning" are not defined

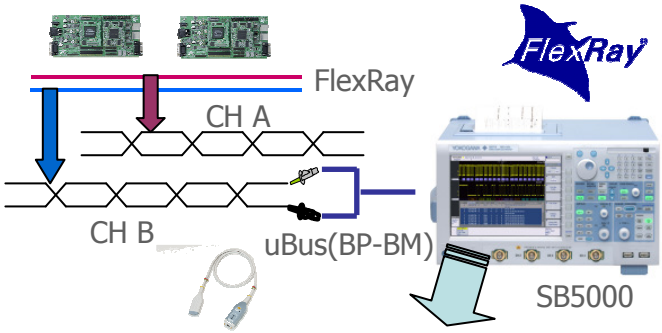
<Figure 5> Signal Voting Variables

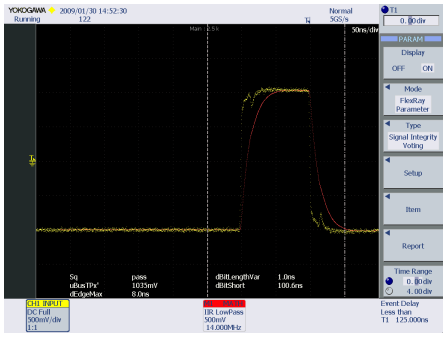
PARAMETER	*dBitLengthVariationMax*	Allowed maximal length variation 7ns
	dBitMin	required minimum duration of the shortest bit at TP4_BDi: 69.95ns @ 10Mbit/s (*) 133.40ns @ 5.0Mbit/s (**) 260.30ns @ 2.5Mbit/s (***)
	uData0Top	required level (top): -330mV
	uData1Top	required level (top): 330mV
	dIdleDetectionMin	minimal timeout to detect *Idle*: 50ns

<Figure 6> Signal Voting Parameter List

SI Voting using the Yokogawa SB5000

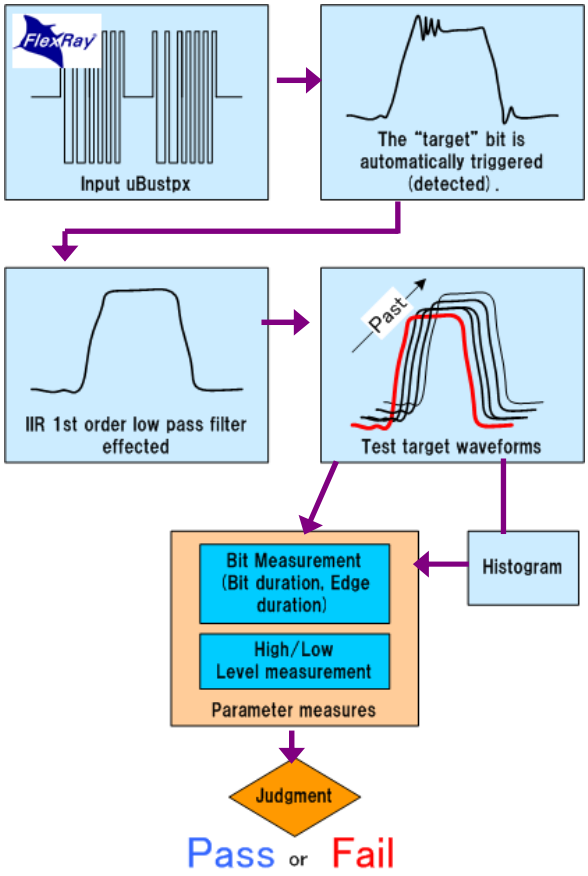
The Yokogawa SB5000 vehicle serial bus analyzer performs the SI voting procedure analysis and judgment as follows.





<Figure 7> Measurement and analysis by the Yokogawa SB5000

As shown in figure 7, the uBustpx differential signal is measured using a differential probe. Figure 8 shows the flowchart of the process inside the SB5000.



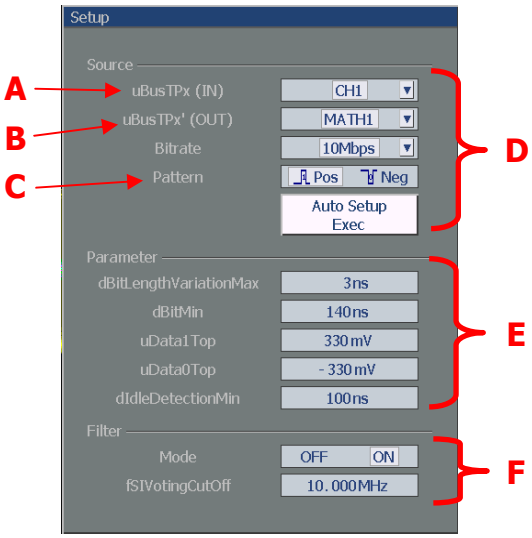
<Figure 8> SI Voting analysis flowchart

The single negative or positive bit (target bit) is automatically captured according to the condition in the setup. The filtered signal (uBustpx') is internally calculated using a IIR, 1st order low pass filter. The original bit waveform (uBustpx) and the filtered version (uBustpx') are displayed simultaneously on a single screen.

The bit duration (dBit for all threshold variations), the edge duration(dEdge01, dFdge10) and the "High" (or "Low") value are measured using the parameter measurement function, then it is judged and the result of "Sq" is displayed.

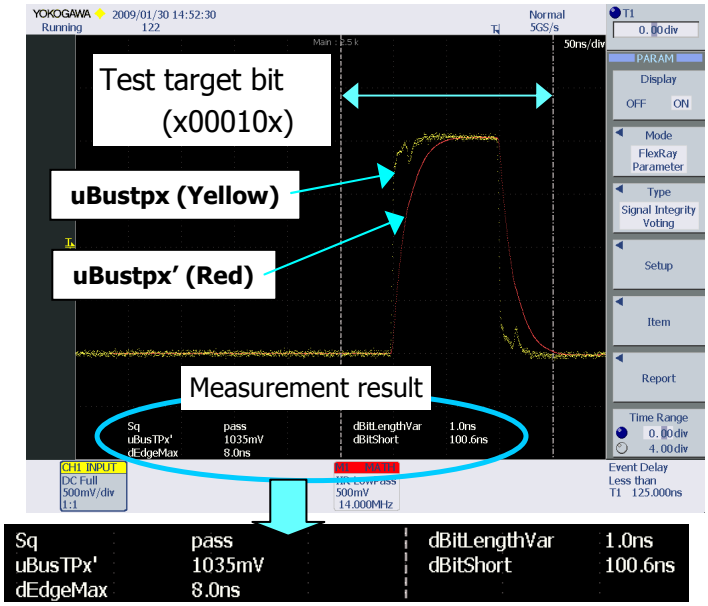
The analysis and judgment are performed continuously in real time whenever the test bit is captured.

Once the conditions shown as A, B and C in figure 9 are set, The other necessary setup configurations are determined automatically.



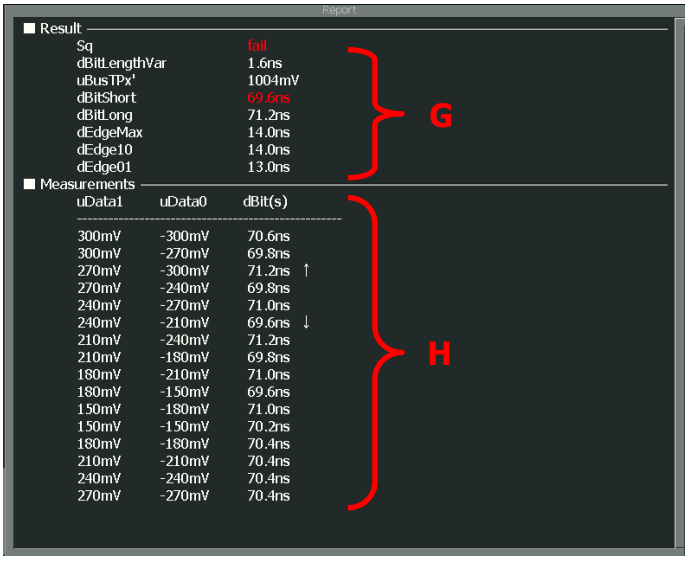
<Figure 9> SB5000 SETUP menu

A: uBustpx: Source waveform
B: uBustpx': Low-Pass-Filtered source waveform
C: Pattern of the target test bit
D: Once A, B and C have been appropriately set, the parameters shown in "E" will be configured automatically when an "Auto setup Exec" is performed. The test target bit is captured as shown in Figure 10 (an example of the "Pos(X00010x) pattern))
E: These parameters can be changed if necessary.
F: The filter can be switched ON or OFF. The cut-off frequency can be adjusted if necessary.



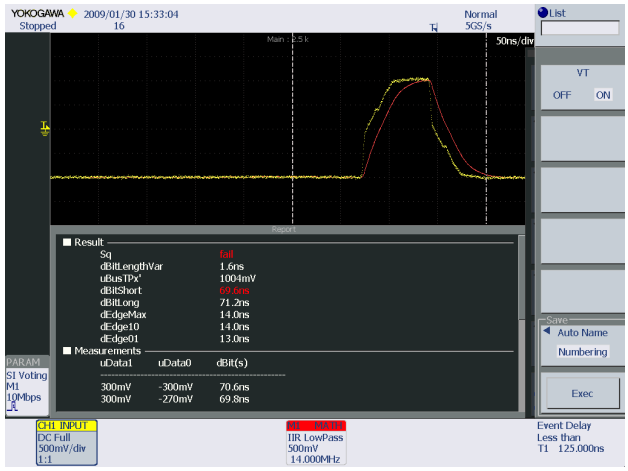
<Figure 10> Analysis Example

The result of "Sq", shown as ⑥ in Figure 2, along with the measurement results of parameters for ⑤ are shown on the screen as a report. (see Figure 11)



<Figure 11> Report display

G: In case of "Fail", the corresponding item(s) is highlighted in red.
H: The measurement result of "Schmitt Trigger" can be displayed (and updated in real time). The Max and Min values are indicated by arrows.



<Figure 12> Simultaneous display of the waveform and the report

The waveform and report can be displayed simultaneously as shown in Figure 12. The report can be saved as a CSV file as shown in Figure 13.

	A	B	C	D	E
1	Measure Type	Signal Integrity Voting			
2	Model Name	SB5000			
3	Model Version	9.99			
4	Result				
5		Sq	fail		
6		dBitLengthVar	1.60E-09	s	
7		uBusTPx'	1.00E+00	V	
8		dBitShort	6.96E-08	s	
9		dBitLong	7.12E-08	s	
10		dEdgeMax	1.40E-08	s	
11		dEdge10	1.40E-08	s	
12		dEdge01	1.30E-08	s	
13	Measurements				
14		uData1	uData0	tdBit	
15		300mV	-300mV	7.06E-08	s
16		300mV	-270mV	6.98E-08	s
17		270mV	-300mV	7.12E-08	s
18		270mV	-240mV	6.98E-08	s
19		240mV	-270mV	7.10E-08	s
20		240mV	-210mV	6.96E-08	s
21		210mV	-240mV	7.12E-08	s
22		210mV	-180mV	6.98E-08	s
23		180mV	-210mV	7.10E-08	s
24		180mV	-150mV	6.96E-08	s
25		150mV	-180mV	7.10E-08	s
26		150mV	-150mV	7.02E-08	s
27		180mV	-180mV	7.04E-08	s
28		210mV	-210mV	7.04E-08	s
29		240mV	-240mV	7.04E-08	s
30		270mV	-270mV	7.04E-08	s
31					

<Figure 13> Report file example

SB5000 Key technologies for performing the SI voting procedure

1. High speed, real time analysis

Thanks to the "ADSE" (Advanced Data Stream Engine) developed by Yokogawa, the whole process can be performed at high speed and in real time. The screen update rate (triggering rate) is also high, so the target signal (bit) is repeatedly captured with minimal dead time. The update rate is practically about 19Hz(Note 3).

Note 3: It is just regarded as reference data.

ADSE (Advanced Data Stream Engine)

2. Ease of use

The "Auto Setup Function" enables the analysis setup procedure to be performed quickly and easily. All setup parameters are visible together on one screen. If necessary, each parameter value can also be adjusted.

3. High speed test results

The test results, including the pass or failure judgment of "Sq" and the parameters, can be displayed on screen and saved as a CSV report file.

SB5000 Detailed Functional Specifications

Setup Setup configuration for the test.

Source
uBusTPx(IN): Source signal before Low Pass Filter(LPF)
uBusTPx'(OUT): Math1(M1) to Math4(M4)
Select the source signal after LPF.
The selected Math signal (waveform) is displayed as a IIR Low Pass (first order) filtered waveform.
Bit rate : Select 10, 5 or 2.5 Mbps
Pattern : Select Pos(x 00010x) or Neg(x 11101x).

Auto Setup Exec: Configuration can be automatically setup for the test.

Parameter
dBitLengthVariationMax: Settable from 1ns to 150ns
dBitMin : Settable from 60ns to 400ns
uData1Top : Settable from 300mV to 900mV
uData0Top : Settable from -900mV to -300mV
dIdleDetectionMin: Settable from 20ns to 200ns
fSIVotingCutOff: Cut off frequency for the LPF (settable from 0.01Hz to 1GHz).

Item	Settings to display the test results and parameter values.
Results	: Sq(Pass/Fail) Test results
Measurements:	dBitLengthVariation /uBusTPx'(Max or Min) [Maximal or Minimal level of filtered waveform] /dBitShort/dBitLong /dEdgeMax[MAX(dEdge01, dEdge10)]/ dEdge10/dEdge01 Parameter values corresponding to the test result.
Report	Test result can be displayed as a report. The displayed contents are: 1. Result - Sq (Pass or Fail) - Cause of Fail (when Sq = "Fail") 2. Measurements- dBitLengthVariation/ uBusTPx'(Max or Min) /dBitShort/dBitLong /dEdgeMax /dEdge10/dEdge01/ Duration of each "Schmitt Trigger"

- The report can be updated in real-time during acquisition.
- The report can be saved as a CSV text file.

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