Emphasizing Serial Bus Signals

Written by Tom Lecklider, Senior Technical Editor

No longer is it just speed that is driving interest in serial buses, according to MaryJane Hayes, product manager for high-volume oscilloscopes at Agilent Technologies. 'Lower-speed serial buses are finding more and more application in today's marketplace. They are widely used in mixed-signal embedded designs for communications among EEPROMs, DACs, and ADCs and devices such as microprocessors, microcontrollers, and DSPs,' she said.

With scope-based serial bus trigger and analysis solutions, you can recognize and trigger on a large number of selectable states on buses such as the inter-integrated circuit (I^2C), serial peripheral interface (SPI), controller area network (CAN), Flexray, and universal serial bus (USB). Further, the captured data may be decoded and displayed in an informative, color-coded format that highlights read address, write address, idle state, and active bus among other conditions.

Joseph Ting, digital oscilloscope product manager at Yokogawa Corporation of America, outlined two primary advantages in using a scope platform to analyze serial bus activity. 'First, a scope can identify waveform quality issues related to analog characteristics such as noise, rise time, or overshoot. By comparison,' he continued, 'a logic analyzer or dedicated protocol analyzer typically can only extract timing or protocol information. Second, a scope's additional channels support time correlation of the serial bus activity with other mixed signals in the system, such as power supply, analog sensor, or memory bus.'

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In contrast to relatively slow I^2C control messages or automotive sensor data, computer and communications system buses are all about speed. Recently, the bottleneck represented by the 132-MB/s top speed of the PCI bus was eliminated by PCI Express (PCIe).

With a 2.0-Gb/s data rate, one lane of full duplex first-generation serial PCIe is almost twice as fast as parallel PCI. In common with many other high-speed standards, 8b/10b encoding is used to improve synchronization and provide a more uniform distribution of high and low states. Of course, encoding reduces the effective bus speed, but up to 16 lanes can be grouped together for multigigabit/s data transfer if required (**Figure 1**).

Figure 1. Invalid Character (SKP-) in a PCIe Compliance Pattern Shown Via 8b/10b Decoding
Courtesy of Agilent Technologies

Different types of computing and communications applications have special requirements, and there is no shortage of serial buses to accommodate them. For example, RapidIO uses source routing to streamline peer-to-peer communications among computer systems. This means that only small, local addresses must be handled by a switch routing table, speeding up data exchange.

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In another example, Infiniband is used to interconnect server memory and I/O devices. Infiniband is particularly efficient in this role because it is hardware based and offloads data communications from the related processors. With characteristics similar to PCIe, Infiniband is an 8b/10b full-duplex network running at 2.5 Gb/s in which lanes can be grouped for even higher data rates.

For many years, peripheral storage devices have interfaced to computers via special-purpose buses. The advanced technology attachment (ATA) standard connected disk drives to computers with a wide parallel cable. More recently, serial ATA (SATA) has provided faster operation with a much simpler interface. The original ATA name was changed to parallel ATA (PATA) to eliminate any possible confusion between the two similar standards.

Also related to disk drives, there have been many revisions to the legacy small computer systems interface (SCSI) bus. One result has been the introduction of high-performance serial attached SCSI (SAS). SAS and SATA disks and cables use the same connectors, and a SATA disk will run on a SAS controller. A SAS disk won't run on a SATA controller, however.

There are many other buses that fall between the speed extremes, such as the very popular USB and the IEEE 1394 or FireWire bus primarily used for audio and video data. Depending on which buses you are working with, your choice of test tools will vary. General-purpose instruments are suitable for some applications, but for high-speed buses, even the fastest logic analyzers require special preprocessing bus probes.

There is no one instrument that addresses the wide range of serial bus characteristics. Even if there were, if it did nothing else, you still would require other equipment to understand how the bus activity related to your system's broader behavior.

Serial Bus Test Equipment

Scopes

Bus physical layer characteristics need to be considered when using any kind of analyzer. Naturally, you have to provide the bandwidth and sampling rate required to capture the signals. For example, PCIe has a 2.5-Gb/s bit rate, which means that the fundamental frequency is 1.25 GHz. Typically, a scope's bandwidth should be at least 5x greater to ensure minimal distortion of the fifth harmonic or 6.25 GHz in this case. This high bandwidth implies that active probes must be used, and above a couple of gigahertz, they become expensive.

High-speed serial bus physical layer analysis involves clock recovery and measurements related to eye diagrams. The Tektronix RT EYE product provides jitter analysis and eye pattern mask testing for standards such as SATA, PCIe, and high-definition multimedia interface (HDMI).

Through 8b/10b decoding on the Tektronix DSA 70000 Series, engineers can work with 8-b symbols rather than the encoded 10-b representations.

Triggering on up to 40 consecutive bits is possible, and data is presented at word level for correlation with physical level waveforms. Similarly, Agilent Technologies' E2680A Serial Data Analysis package for the company's DSO80000 Scopes decodes 8b/10b data in real time and tracks an eye diagram failure back to the data stream that caused it.

Yokogawa's serial bus analysis scopes include serial bitstream trigger and serial cursor capabilities. These features allow you to analyze any serial bus at a binary level. The user can decode or set any string of up to 128 0s and 1s and trigger at a specified bit rate. Both synchronous and asynchronous operations are supported.

One of the more difficult problems affecting high-speed buses is high-frequency signal component amplitude reduction caused by the transmission channel. Intersymbol interference (ISI) or the interaction of one bit with later bits in the sequence results from amplitude and phase distortion caused by the channel. Pre-emphasis increases the amplitude of the first bit in a string of consecutive 1s or 0s to counteract the channel's losses. The term de-emphasis also is used but is the same difference in amplitude referred to the second bit being smaller than the first rather than the first being larger than the second.

With tools such as RT EYE, you can differentiate between an eye diagram with pre-emphasis and one without by including only transition or trailing bits, respectively. Sampling scopes, such as the Tektronix DSA8200, can provide more precise eye diagram analysis by evaluating the effect of noise as well as timing jitter. The 80SJNB software application predicts bit error rate (BER) levels using this technique.

SyntheSys Research produces a range of BERTScope' S Eye Openers that de-emphasize trailing bits in a series of NRZ data bits. The passive devices reduce the amplitude of bits following a transitional bit by an amount defined in the particular bus specification. PCIe 1.0, SATA 1.5 Gb/s, and SATA 3.0 Gb/s standards require 3.5 '0.5 dB, but 6.0 '0.5 dB is needed for PCIe 2.0 and FB-DIMM-1 buses.

High-speed bus interconnects can be characterized by their scattering (S) parameters. Long used to specify microwave components, S parameter characterization recently has been added to the SATA and PCIe specifications. You can use a vector network analyzer from Rohde & Schwarz, Agilent, or Anritsu or take advantage of the time-domain reflectometry (TDR) capabilities of newer sampling scopes. For example, the Textronix DSA8200 with the appropriate TDR module provides a 70?dB dynamic range and up to 50-GHz bandwidth.

For slower buses, built-in bus trigger recognition and data decoding operate not at the physical layer but higher up the protocol stack at the data link layer. Specifically, the medium access control (MAC) sublayer controls things like frames, data encapsulation, and acknowledgement. A scope with bus

triggering and decode capability recognizes the different types of fields within a frame to extract data, address, and control values. Once recognized, these events can be used as triggers or specially formatted in a trace display.

Today, scopes are available with 16 to 36 digital channels as well as the usual two or four analog inputs. These mixed-signal oscilloscopes (MSOs) are ideal for troubleshooting embedded designs that often involve serial buses. With an MSO, you can investigate relationships among analog signals, digital addresses and data, and bus commands.

Agilent's 6000 Series Scopes feature hardware accelerated decoding for I^2C and SPI buses, resulting in very high throughput. In addition, this capability supports troubleshooting random and intermittent errors as well as signal-integrity problems.

Mike Hertz, field applications engineer at LeCroy, explained that the company's scopes 'can decode any combination of SPI, I^2C, CAN, local interconnect network (LIN), FlexRay, UART, RS-232, and 8b/10b serial bus data across any of the four input channels. The user can decode CAN on channel 1, FlexRay on channel 2, 8b/10b PCIe on channel 3, and UART on channel 4. Alternatively,' he clarified, 'the user could decode four different CAN networks across channels 1 through 4 with each operating at a different bit rate.'

In an MSO, it's tempting to use digital channels for bus analysis, and in most scopes, you can do this for buses such as SPI and I^2C. This capability is advantageous because you may need to use the conventional channels for truly analog signals. Nevertheless, digital channels on all MSOs are single-ended inputs with much different impedance and frequency response characteristics than the scope's analog channels. Generally, you shouldn't have a problem, but it could be useful to compare the behavior of a bus when connected to either type of probe just to make sure.

Logic Analyzers

To extract higher-level meaning from serial data, you need to use a logic analyzer or protocol analyzer. Logic analyzers are general-purpose tools so they can be applied to problems other than serial buses. Further, logic analyzers support multibus correlation so you can relate commands on one type of bus to activity on another.

A preprocessing probe often is required, especially for fast buses, but the probes and their associated logic analyzer present a similar user interface for each protocol. This helps to improve productivity and avoid operator errors. The probe handles field recognition and serial-to-parallel conversion requirements much more efficiently than the logic analyzer can and provides a customized connection to the bus.

The FuturePlus Systems FS4405 PCIe Serial Protocol Preprocessor is a good example. This device nonintrusively probes a PCIe bus running at the full 2.5-

Gb/s rate and intercepts various combinations of up to eight channels out of the possible 16. According to the datasheet, 'The probe acquires serial data, converts it to parallel form, recognizes and filters packets, and clocks the information into the [Tektronix] logic analyzer.' In this case, although the preprocessor hardware can filter and trigger on the serial information, the software supports use of the logic analyzer-based trigger functions (**Figure 2**).

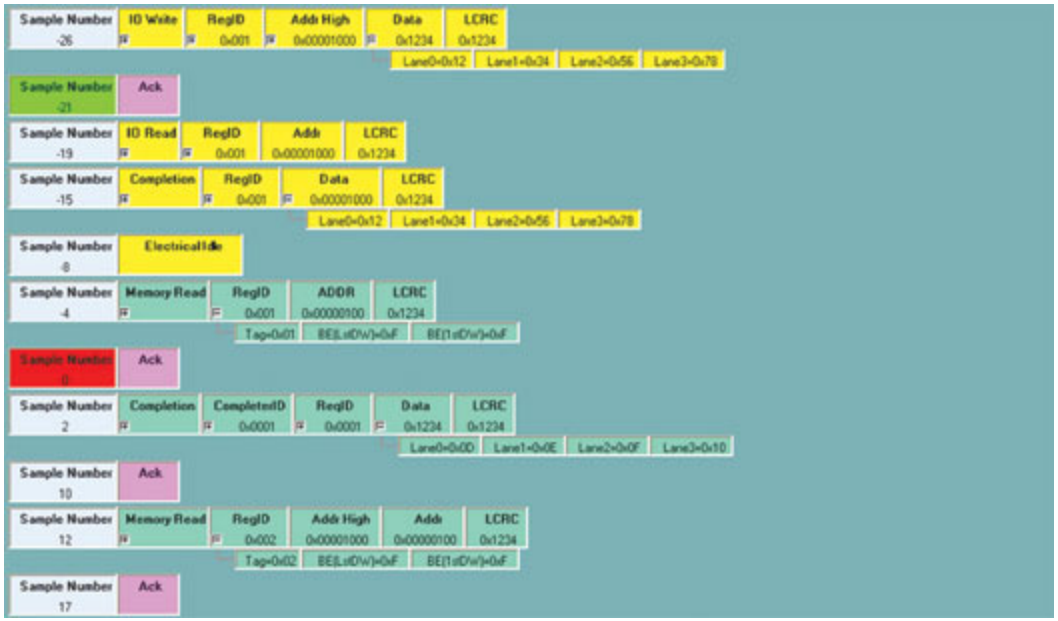


Figure 2. Protocol Analysis Organized in Order of Transactions
Courtesy of FuturePlus Systems

David Grabove, marketing communications manager at FuturePlus Systems, said, 'Current PCIe buses usually are accessible through slot-connected interposer probes. However, the second-generation PCIe specification calls for a doubled clock rate, so future designs may run faster than the reliable limit of such probes. Furthermore, serial buses such as RapidIO don't use any external connectors. For these situations, a connectorless mid-bus probe or other attachment scheme must be used.'

Establishing a nonintrusive bus connection is not a simple matter. The mid-bus probe referred to typically uses spring-loaded contacts to press against a PCB connector pattern that was designed in for this purpose. The bus traces are routed as microstrip lines on the PCB, and the connector pads appear as small disruptions on the lines. This approach eliminates the much larger reflections and distortion an actual physical connector would cause. Of course, it avoids the cost of the connector, too.

Another preprocessor probe is made by Crescent Heart Software. The ATM-1 actually is a serial trigger probe for use with scopes, but it also has optional

protocol analysis capability when used with a Tektronix logic analyzer. The ATM-1 addresses automotive CAN and LIN bus systems. In addition, the company provides serial bus analysis preprocessors for USB and SATA systems.

FuturePlus also makes preprocessors for use with Agilent Technologies logic analyzers. The FS4100 USB Analysis Probe converts the serial data to a parallel form similar to the PCIe preprocessor. All USB cycles and transaction identifiers are decoded and presented as separate bits to the logic analyzer. This approach makes it easy to store all USB traffic, store only certain packet types, or only packets to and from certain locations.

The low-cost GoLogic' PC-based Model U36-1M Logic Analyzer from NCI Logic Analyzers is available with 36 or 72 channels and features 500-MHz asynchronous timing and a 125-MHz transition or state clock rate. In addition to a range of basic logic analyzer functionality, it also provides serial data bus analysis.

'Like any logic analyzer-based solution, the GoLogic captures and displays the raw serial bus signals,' explained Brian Bledsoe, a computer engineer at NCI. 'Our software then converts the raw data to parallel values and displays the formatted data alongside the timing diagrams. The unit can trigger on I^2C and SPI address and data values. Time-based buses such as RS-232, and CAN and LIN in the future, are decoded, but the logic analyzer hardware does not currently support triggering.'

Protocol Analyzers

You may be asking, why should I use a protocol analyzer when a logic analyzer can do the job? That's a fair question, and especially if you already own a logic analyzer, you should check the availability of suitable preprocessor probes before deciding.

Daniel Jackson, president of Crescent Heart Software, explained the choice of instruments this way: 'Although a logic analyzer-based environment provides a standardized high-level GUI, it is our experience that detailed protocol-specific information is best presented and displayed in a bus-unique manner as appropriate for the specific serial bus of interest. Probing a given bus certainly requires a bus-specific connection and interface arrangement even though a logic analyzer would appear at first glance to be ideal for establishing bus-agnostic connection to the system under test.

'In practice,' he continued, 'each serial bus standard is sufficiently specialized or operates at a sufficiently high speed that bus-specific interface hardware must be used to make the connection as well as preprocess bus transactions for presentation to the logic analyzer. The logic analyzer triggers on the information presented to it and disassembles the data to provide a meaningful test display of bus activity.'

Mr. Jackson's views underline the many differences that exist among serial

buses. Manufacturers of dedicated protocol analyzers would agree with his comments and add that their products can provide a greater depth of bus-specific features because they are not constrained by a host logic analyzer.

It can be debated which type of solution makes the better serial bus analyzer, but an undisputed advantage of dedicated protocol analyzers is optional use as a bus exerciser. Logic analyzers are not signal sources and do not provide bus endpoint or root complex emulation. If you need to generate test packets, inject known errors, and perform rigorous compliance testing, a protocol analyzer with exerciser capabilities is a must.

The Catalyst Enterprises SPX Series of PCIe instruments includes analyzers, exercisers, and compliance test suites. Various models address from one to 16 lanes with combined or separate analyzer/exerciser functions. The single-lane SPX-1A Analyzer can be field-upgraded or factory configured to include exerciser capabilities, but the SPX-8E and SPX-8A are separate eight-lane exerciser/analyzer or analyzer-only boards.

The exercisers include capture, trigger, and analysis functions and offer the following features:
' Integrated filter, trigger, and capture display
' Error injection
' Real-time performance analysis
' Statistical traffic analysis
' Ethernet and USB 2.0 host interface
' SpekCheck' compli'ance test (optional)
' Protocol error detection
' Record and playback
' Polarity reversal
' Configuration space decodes
' Scramble and nonscramble options
' Nonstandard link speed support
' Spread spectrum clocking (SSC)
' External triggers in/out
' COM API for programmatic control (option)

The Pro SPX product provides basic capabilities while the Expert SPX has basic and advanced functionality.

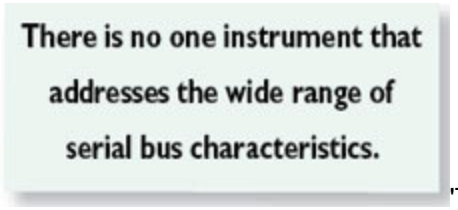
In addition to probes and software for conventional logic analyzers, Agilent also offers stand-alone protocol analyzers. The Model E2960A combines PCIe analyzer and exerciser functionality. As presented in the datasheet, 'Combined traffic generation and protocol analysis dramatically increase your test coverage to reduce the risk of costly redesigns and recalls.'

The analyzer uses either a two-slot or four-slot chassis that houses serial I/O modules. Featuring an FPGA-based design, the modules support upgrades and exerciser or analyzer functionality. A variety of modules addresses different bus types. For example, the 173x Series of test cards deals with

Fibre Channel SAN applications, the E2960B modules cover both PCIe 2.0 at 5 Gb/s as well as PCIe 1.0 at 2.5 Gb/s, and E2980A modules are used with the Advanced Switching Interconnect (ASI) bus.

Triggering capabilities, as you might expect, are very sophisticated in this type of protocol analyzer. For the E2960A, a graphical representation keeps track of the trigger logic you have assembled in a drag-and-drop fashion from a mix of elements such as counters, states, and patterns and actions including store, increment counter, and trigger out. Further, multiple analyzers can share events for cross-triggering.

Up to 15 different protocols are supported by Finisar's Bus Doctor Analyzers through the addition of plug-in modules. Basic logic analyzer operations also are provided. This comprehensive approach is claimed to be necessary for engineers developing consumer electronics devices.



'The Bus Doctor displays high-level dialogs and event filters, allowing engineers to home in and capture and analyze the hardware and software errors,' said Steve Wong, the company's Network Tools Division product marketing director. 'Bus Doctor eliminates the need for multiple testing tools so consumer products can be efficiently developed. For example, designers of SATA solid disk drives need to observe flash memory activity using logic analysis and then correlate that to SATA data using a serial bus analyzer.'

Mr. Wong explained that serial protocols send two types of messages: primitives to negotiate speed and flow control and frames that contain data such as commands and responses. The Bus Doctor presents these two types of information in a similar fashion on its GUI regardless of the bus type that is being probed and decoded.

Clearly, this reduces a user's learning curve. In addition, captured hybrid data can be presented in a common format. In the development of a video camcorder with a USB link and a SATA drive for storage, the primitive and frame flows from both buses are shown on a single display in a time-ordered sequence.

LeCroy's range of protocol analyzers and exercisers includes models for several serial buses. For example, the Avalanche' SAS analyzer simultaneously monitors and records activity from four SAS links. Features include real-time hardware-based triggering and filtering for either 3- or 6-Gb/s systems. The Frame Tracker Display, a summary view, shows transport level events in a time-synchronized table format.

With the company's SASTracer/Trainer', you get both an analyzer and exerciser with one, two, or four recording channels and the capability to display multiple protocol traffic by synchronizing to other types of LeCroy bus analyzers. Additional tools extend your SAS solutions: SASTracker' debugs command timeout problems, SAS InFusion' injects errors and modifies traffic in SAS and SATA systems, and the Compliance Test Suite for SAS uncovers latent compliance problems before a device enters production.

Summary

Serial bus analysis is a large topic with both physical layer aspects as well as higher level protocol issues. As the varieties of buses and their speeds continue to increase, so too does your choice of appropriate test instruments. Several products have been highlighted to help make you aware of the types of measurement solutions available.

If you are working with serial buses already, you are familiar with some of the test instrumentation on the market. If serial data systems are new to you, perhaps this article will resolve some of your questions. Much more information about serial bus operation, troubleshooting, and test tools can be found on the websites of the major test and measurement manufacturers.

Viewing High-Speed Differential Signals

PCIe signals are transmitted dif'ferentially on two pairs of wires, one pair for each direction. The best probing solution is to use a true differential probe that eliminates the bus's common-mode voltage at the probe input and requires only one scope channel.

However, such probes have common-mode voltage limits, and it's possible to exceed the common-mode rating even if the differential voltage is within range. This kind of overload may result in clipping, but it also can cause signal distortion without obvious clipping, a very subtle kind of measurement error.

Lacking a differential probe, many engineers would connect two active analog scope probes to two input channels. By subtracting the signals from each other, the action of the differential probe can be approximated. This method works but can cause confusion. How well it works depends on the gain and frequency response matching of the two channels and probes.

The maximum amplitude that can be applied without clipping is limited by a channel's ADC. For example, assume you want to see a PCIe bus 0.4-Vpk-pk differential signal with a resolution of 0.1 V/div, and your scope's ADCs allow 10 divisions vertically; that is, they cover the usual '4 divisions either side of center ' another over-range division. What is the maximum permissible common-mode voltage if you DC couple the signals?

With both channels set to 0.1 V/div, you would see a '0.4-Vpk-pk resultant centered vertically if each signal had a '0.2-V amplitude. However, the maximum signal amplitude the ADCs will handle without clipping is '0.5 V.

Figure A shows a pair of differential signals centered in the ADC range, and it follows that the common-mode voltage must lie between '0.3 V. For PCIe, the nominal high and low voltages are 1.2 V and 0.8 V, respectively, giving a 1.0-V common-mode value. You can accommodate higher common-mode voltage but only at reduced resolution. So, in this case, you would need to use 0.5-V/div vertical sensitivity to avoid clipping.

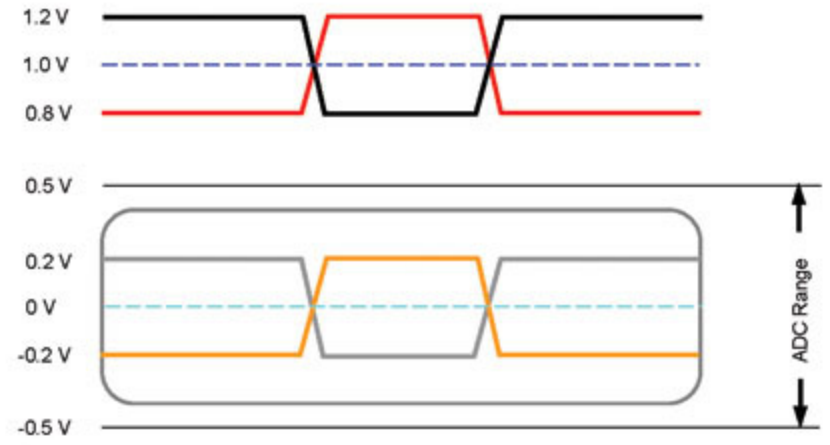


Figure 3a.

Figure A. PCIe Signal Levels Relative to Scope Input Range

The display you would see under these conditions is shown in **Figure B.** The maximum 1.2-V signal level has been accommodated, but the pk-pk excursions are small.

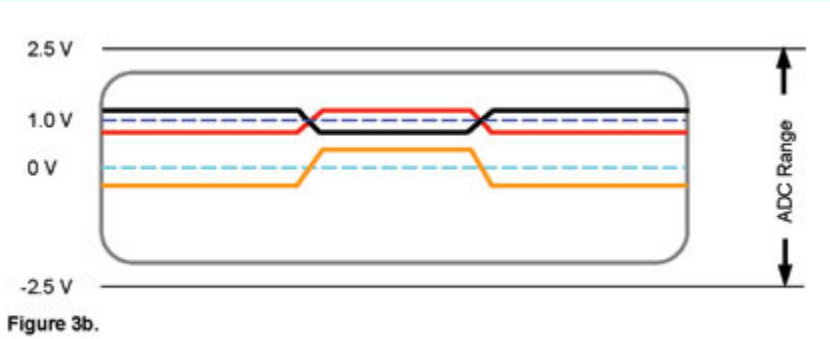


Figure 3b.

Figure B. PCIe Signals Displayed at 0.5-V/div Sensitivity

A LeCroy application brief, *Splitting the Grid*, discusses the relationship between accuracy and signal amplitude in DSOs. Basically, you lose accuracy by restricting the dynamic range of a signal, either because of common-mode limitations as in this case or when amplitudes are deliberately reduced to compare two or more traces simultaneously.

Most modern scopes provide a true offset capability rather than shift. Both offset and shift reposition the trace, but offset does so by cancelling a portion of the signal's DC component. So, if you can offset the two PCIe inputs by -1.0 V, as shown in **Figure C**, the '0.4-V signal resulting from the subtraction process can be viewed at a 0.1-V/div sensitivity, maximizing measurement accuracy.

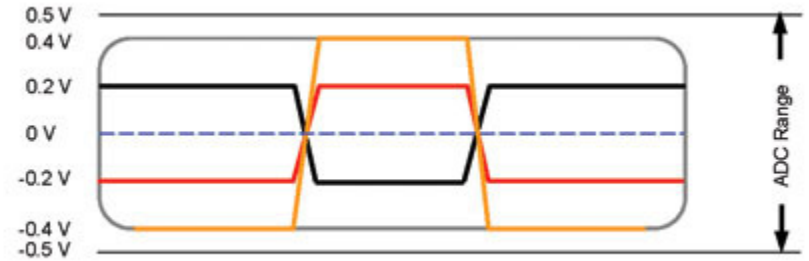


Figure 3c.

Figure C. PCIe Signals Offset and Displayed at 0.1-V/div Sensitivity

In contrast, applying trace shift fol'lowing a channel's ADC only affects the displayed trace position. An offset capability also may be available on active probes, so care must be used in deciding where and how much offset to apply.

FOR MORE INFORMATION		
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