AP9945 AND AQ2200-601 10-GBIT/S COMPACT BIT ERROR RATE TESTERS

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With improvements in the speed and bandwidth of communication networks in recent years, 10-Gbit/s high-speed optical communications systems are becoming increasingly widespread in core networks, as well as access networks and LANs. Accordingly, devices and modules for use in 10-Gbit/s transmission are being actively developed, causing increasingly fierce price competition. Under these circumstances, the bit error rate testers (BERT) necessary to test these devices and modules are also facing a demand for lower prices. We have explored essential functionality and performance and examined product specifications, with a focus on application to the production of optical transceivers. Consequently, we have developed two compact and economical 10-Gbit/s BERTs, a plug-in module model and a portable model, featuring variable amplitudes, cross-points and voltage offsets for the data output and a built-in clock and data recovery (CDR) function.

INTRODUCTION

With the move to faster and larger capacity communication, 10-Gbit/s synchronous optical network/synchronous digital hierarchy (SONET/SDH) transmission systems have already been commercialized for core networks, and with improved device technology in recent years and use of 10-Gbit/s transmission even by CMOS technology, 10-Gbit/s transmission has also been expanding into access networks as costs decrease. Since FTTH services are becoming widely available and communication carriers are beginning to reinvest in optical transmission equipment, it can be said that access networks are also entering the gigabit era. In this environment, the new 10-Gbit/s band communication systems are doing well in the market. For example, the 10-Gbit Ethernet, standardized by IEEE 802.3ae in 2002, allows efficient utilization of communication traffic in comparison with SONET/SDH and has good compatibility with the Internet. Fibre Channel is a storage interface very similar to Ethernet. Also, for frames to which forward error correction (FEC) like an optical transport network (OTN) has been assigned, long-distance communication can be compatible with high quality. However, each of these communication systems has adopted its own bit rate as shown in Table 1.

For 10-Gbit/s transmission, optical communication is a prerequisite, and there are multiple industry standards known as multi-source agreement (MSA) for optical transceivers, or optical-electrical converters. With the aim of increasing the share of adopted MSA, transceiver vendors have been proceeding

Table 1 10-Gbit/s Band's Bit Rates

Communication System	Standard Bit Rate	FEC Bit Rate
SONET/SDH	9.95328 Gbit/s	10.664 Gbit/s
Ethernet	10.3125 Gbit/s	11.0957 Gbit/s
Fibre Channel	10.519 Gbit/s	11.318 Gbit/s
OTN	10.709 Gbit/s	

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Figure 1 AQ2200-601 Module-model BERT (Installed in Frame Controllers)

Figure 2 AP9945 Portable BERT

quickly with the development of optical transceivers compatible with multiple bit rates to support multiple noted communication systems.

Currently, we have developed two models of the 10-Gbit/s bit error rate testers (BERTs): a plug-in module model mainly targeted at mass-production testing of optical transceivers, and a portable model mainly targeted at researchers' or developers' second machines. Figure 1 and 2 show the external views of these testers.

BERT

The bit error rate measured by the BERT is a ratio of error bits to measured bits and is used as an indicator for representing the quality of devices, modules, or networks. For example, for a 10-Gbit/s SDH, the ITU-T G.691 specifies the minimum optical-receiving sensitivity at a bit error rate of 1×10^{-12}, and the bit error rate must be better than 1×10^{-12} at the optical-receiving power specified in this standard. The bit rate of this SDH is 9.95328 Gbit/s and 9,953,280,000 bits of data are transmitted per second. If an error occurs at a ratio of one bit per second, the bit error rate is 1/9,953,280,000 = 1.004694×10^{-10}. Therefore, if an error occurs at a ratio of one bit per 100 seconds, the bit error rate becomes 1.004694×0^{-12}, while if no bit of error occurs during a measurement of 100 seconds or more, it can be determined that the SDH concerned has a quality better than 1×10^{-12}. The BERT is an instrument which measures this bit error rate (BER).

CONFIGURATION

This section describes the circuit configuration of the 10-Gbit/s BERT and its operations.

The AP9945 and AQ2200-601 have a significantly different appearance because they have different platforms. However, as BERTs, they share in common the same circuit configuration and main components. The following describes the BERT taking AQ2200-601 as an example.

Figure 3 shows the circuit block diagram of the AQ2200-601 10-Gbit/s BERT Module.

Many conventional BERTs consist of two separate enclosures: a pulse pattern generator (PPG) that generates signals

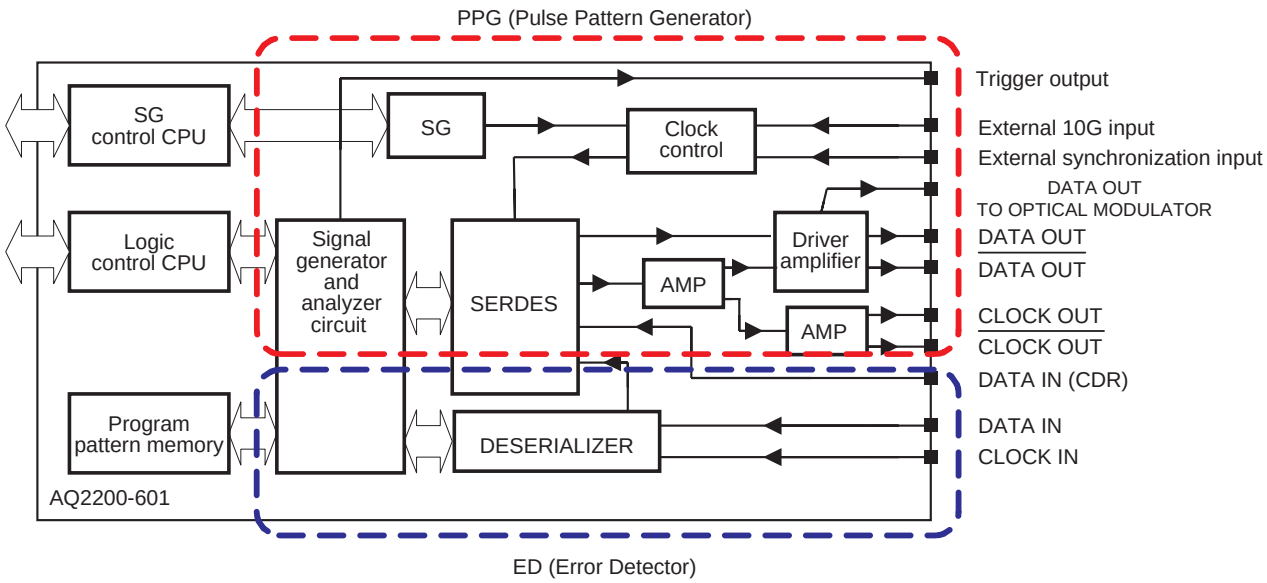

Figure 3 AQ2200-601 Circuit Block Diagram

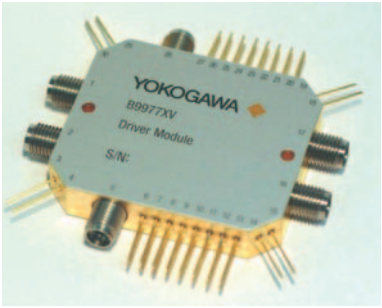

Figure 4 External View of the Driver Amplifier

and an error detector (ED). The BERTs developed by Yokogawa this time, have integrated the PPG and ED sections into one piece to achieve improved integrity and compactness.

First, the signal generator (SG) generates a clock of 621.8 MHz to 707.5 MHz, 1/16 of the bit rate. This SG employs a fractional frequency-dividing PLL, allowing frequency to be variable in 62.5 Hz increments. This frequency is equivalent to the variable width of 1 kHz increments when it is subsequently multiplied 16 times to 9.95 GHz - 11.32 GHz. A clock output from the SG is input to SERDES to be multiplied 16 times to a clock of 9.95 GHz - 11.32 GHz and is then used as a system clock. The SERDES stands for a serializer and deserializer and has a function for multiplexing a parallel signal into a serial signal and a function for separating a parallel signal from serial signals. A system clock output from the SERDES is passed through AMP and output to CLOCK OUT on the front panel. Furthermore, a clock obtained by 1/16-frequency dividing a system clock is also output from the SERDES and passed to the signal generator/analyzer circuit. In response to this 1/16-frequency divided clock, the signal generator circuit generates a measurement pattern and outputs it as 16 parallel signals to the SERDES. The SERDES multiplexes these 16 parallel signals into a serial signal and outputs it to the driver amplifier. The driver amplifier wave-shapes this signal using D-FF, varies its amplitude in the AMP circuit, applies cross-point variation, and varies the offset voltage in the offset circuit. It then outputs the signal to DATA OUT on the front panel. The above is an explanation of the PPG's operations.

Table 2 Main Specifications of the AQ2200-601

Overall	Clock mode	Internal and external clocks and external reference
	Internal clock resolution/accuracy	1 kHz/±3 ppm
	Bit rate	9.95 Gbit/s to 11.32 Gbit/s
	Measurement patterns	PRBS, PROGRAM, SDH/SONET (optional)
	PRBS* pattern length	2^7–1, 2^9–1, 2^{10}–1, 2^{11}–1, 2^{15}–1, 2^{23}–1, 2^{31}–1
	PROGRAM pattern length	16 to 256 bits/bit step, 256 to 64 Mbits/128-bit step (optional)
	Trigger output	1/16, 1/64, pattern
	Remote interface	GP-IB and LAN
	Dimensions	94(W)×117(H)×321.5(D)mm
	Weight	2.6 kg or less
PPG	Data output amplitude	0.5 Vp-p to 2.0 Vp-p/0.01 V step
	Offset variable	-2.0 V to +3.0 V/0.01 V step
	Cross-point variable	30% to 70%/1% step
ED	CDR function	Compatible input (DATA IN1), non-compatible input (DATA IN2)
	Input sensitivity	100 mVp-p or less
	Threshold variable	±0.35 V/1 mVstep(DATA IN1), ±0.3 V/1 mVstep(DATA IN2)

*PRBS: Pseudo random binary sequence

In contrast, the ED measures a data pattern input to DATA INs. This 10-Gbit/s BERT has two DATA INs on the front panel. Data input to one of the DATA INs by the clock and data recovery (CDR) function in the SERDES is timing-adjusted based on a clock reproduced by the CDR and is then separated into 16 parallel data. These 16 pieces of parallel data are passed together with a clock obtained by 1/16-frequency dividing a CDR-reproduced clock to the analyzer circuit for error measurement. Data input to the other DATA IN that has no CDR function is separated, together with a clock input to the CLOCK IN, by the dedicated deserializer into 16 parallel signals, which are then measured for error(s) in the same way by the analyzer circuit.

The driver amplifier described in the PPG section is a hybrid IC using the ultrahigh speed compound semiconductor developed by Yokogawa Electric for the 10-Gbit/s BERTs. Figure 4 shows the external view of the driver amplifier. Figure 5 shows the driver amplifier circuit configuration. This driver amplifier consists of the D-FF, AMP, and offset circuits and has been integrated into a compact metal case as small as 44.5×33.5×8.4 mm with the noted functions incorporated.

The 10-Gbit/s BERTs developed this time can adopt commercially available ICs for the SERDES by limiting the bit rate range to the 10 Gbit/s band only. Also, because the in-house driver amplifier has integrated several commercially available devices into one device, coaxial wiring between them has been eliminated, enabling the BERTs to achieve compactness and low costs.

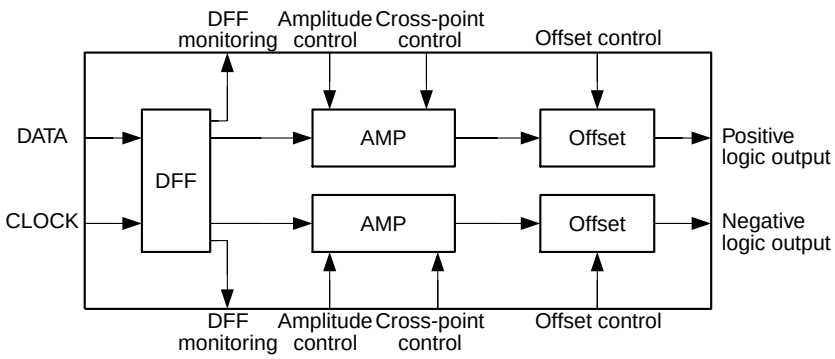

Figure 5 Driver Amplifier Circuit Configuration

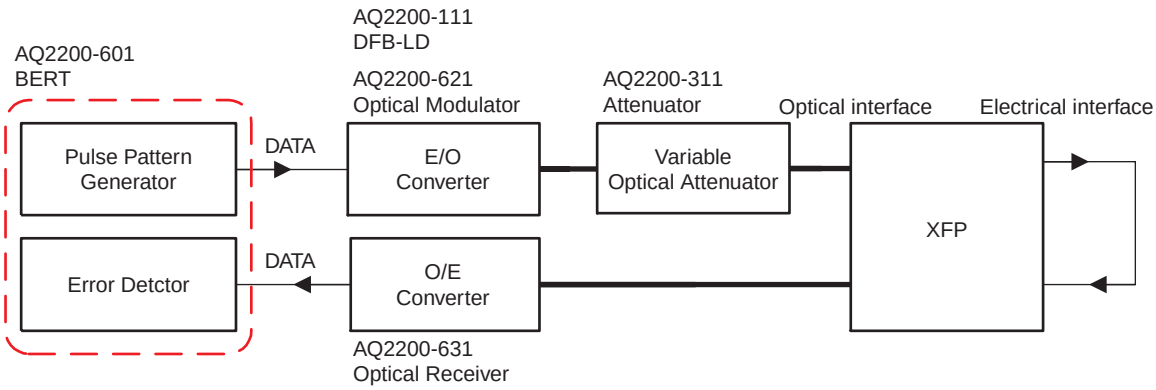

Figure6 Example of Connection between the BERT and DUT

MAIN SPECIFICATIONS

Table 2 shows the main specifications of the currently developed AQ2200-601.

APPLICATIONEXAMPLES

As an example of connection between the BERT and the device under test (DUT), an example of connecting the AQ2200-601 to the XFP transceiver module's optical interface using an E/O converter and O/E converter is shown in Figure 6.

A DATA signal output from the pulse pattern generator (PPG) is converted into an optical signal by the E/O converter, passed through the optical attenuator, and connected to the XFP's photoreceiver. The optical signal input to the XFP's photoreceiver is converted into an electrical signal, which is output to the transmitter side interface. This signal is then loopback-connected to the electrical input of the XFP's photo-transmitter. Then, the same bit pattern as the input optical signal is output from the XFP's optical output section. This output bit pattern is converted into an electrical signal by the O/E converter and then measured by the error detector (ED). In general, error detectors require a CLOCK input, but since this 10-Gbit/s BERT incorporates CDR, simply connecting only a DATA input allows the instrument to perform error measurements.

In these conditions, using the variable optical attenuator to adjust the XFP's optical input level allows the BERT to obtain the error rate characteristics with respect to the optical input level. The results of this measurement primarily represent the optical-receiving characteristics of the photoreceiver. Here, the measured data obtained by connecting an output of the optical attenuator directly to the O/E converter is shown in Figure 7. It is apparent from the figure that a optical-receiving sensitivity of -15 dBm was obtained at a bit error rate of 1×10^{-12}.

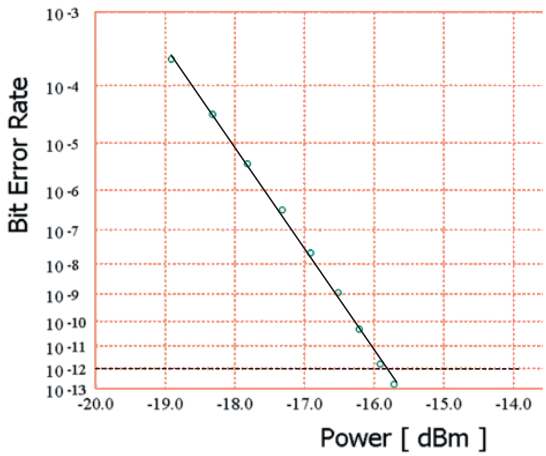

Figure 7 Optical-receiving Sensitivity Characteristics of the Bit Error Rate

CONCLUSION

We hope that these two models of the 10-Gbit/s BERTs developed by Yokogawa this time are of help to users. From now on, we wish to add functions which will meet stronger market demands, such as supporting SONET/SDH frame patterns, to upgrade the BERTs to be even better products. ◆

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